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10/566,011	01/25/2006	Josef Baumgartner	2003P0850WOUS	9957

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SIEMENS CORPORATION
INTELLECTUAL PROPERTY DEPARTMENT
170 WOOD AVENUE SOUTH
ISELIN, NJ 08830

EXAMINER	
AKBAR, MUHAMMAD A	
ART UNIT	**PAPER NUMBER**
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,011	BAUMGARTNER ET AL.	
	Examiner	Art Unit	
	Muhammad Akbar	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim(s) 20-29 and 32-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujioka et al (U.S. Patent No. 5,212,373).

Re claim 20, Fujioka discloses a method for reducing the power consumption (see abstract) of a non-contact (i.e.contactless) IC card device (20 of fig.2) i.e. mobile data memory for data transmission with a external device (i.e. external device is able to communicate (transmit/receive) with non-contact IC card through antenna (42 of fig.2) via radio wave (91 and 92 of fig. 2),therefore external device essentially functioning like read/write device) comprising: providing a battery component (6 of fig.2) for energy store and energy consuming components includes central processing unit (CPU) (31 of fig.2), read only memory (ROM 32 of fig.2),random access memory(RAM 33 of fig.2), oscillator circuits (1, 2 of fig.2), input/output circuits (34 of fig.2), modulating/ demodulating circuits (41 of fig.2) and antenna circuits (42 of fig.2) for the non- contact IC device (mobile) data memory(see fig.2-4, col.3 lines36-63); supplying the non-contact IC card (mobile) data memory by applying command of CPU,ROM,RAM during the standby operation mode [i.e. cycle inactive idle mode] (i.e. in the standby operation

mode, in response of command given by CPU, the clock is disable for resumption of operating voltage to the analog circuits)(see col. 2 lines 59-68-col.3 lines1-21); and supplying a first clock generating a lower frequency clock signal from a first oscillator; and supplying a second, higher clock frequency from a second oscillator for data reception during standby operation mode for reducing power consumption(see fig. 2-3, col.2 lines 20-25).

Re claim 21, as discussed above with respect to claim 20 and Fujioka further discloses in response of the external devices key input or signal input (i.e. during IC device receives signal from the external device) the second clock is generated higher frequency for demodulating the received signal by the trigger signal demodulating circuits (41 of fig.2) thus, reducing power consumption in standby mode (see col.2 lines 21-25) [i.e. higher clock frequency is used for data demodulation of a received signal].

Re claim 22, as discussed above with respect to claim 21 and Fujioka furthermore discloses the CPU (31 of fig. 2) to make a judgment whether the received (transfer (i.e. transmit or receipt data) between IC card and external device) data signal is normal or error (at step S5 of fig.4) [i.e. the level of receiving signal is measured] and execute predetermined processing and output result processing (at step S6-S7 of fig.4) by using input/output control circuits (34 of fig.2) and internal clock circuits (36 of fig. 3) for iteration [i.e. cyclic polling time](at step S8 of fig.4); and if the judge (step S5 of fig.4) found receives data signal wrong or error or data is being transferred (i.e. received)

inappropriately the CPU(31) perform error processing (step S9 of fig. 4) and further processing execute (step S8 of fig.4) to turn off the internal clock inhibit circuits(36 of fig.2) and demounted data by demodulating circuits (43 of fig. 2) (see fig.2-4, col.5 lines 3-41) [i.e. level of the received signal is measured within the cyclic polling time and the received signal is then data demodulated if a minimum level is present].

Re claim 23, as discussed above with respect to claim 22 and Fujioka furthermore discloses when the received data signal is normal (at step S5 of fig.4) execute predetermined processing and output processing is completed (at step S6-S7 of fig.4) and CPU sends commands to turn off the switch circuits (11 of fig.2) and device is operated in standby mode (see fig.3-4 col.5 lines 16-41) [i.e. second clock frequency is switched off again if a minimum level is not present].

Re claim 24, as discussed above with respect to claim 21 and Fujioka furthermore discloses when the data demodulation of the received signal is completed (ended) by demodulating circuits (43 of fig. 2) if the CPU read data is error i.e. invalid (see fig.2-4, col.4 lines 46-60 and col.5 lines 3-41).

Re claim 25, as discussed above with respect to claim 24 and Fujioka furthermore discloses if the judge (step S5 of fig.4) found receives data signal wrong or error or data is being transferred (i.e. received) inappropriately [i.e. CPU data read invalid] the CPU (31) perform error processing (step S9 of fig. 4) and further processing

execute (step S8 of fig.4) to turn off the internal clock inhibit circuits (36 of fig. 3) and switching circuits(11 of fig.2) for returning standby mode (see fig.2-4, col.5 lines 3-41) [i.e. the second clock frequency is switched off again if invalid read data is present]

Re claim 26, as discussed above with respect to claim 21 and Fujioka furthermore discloses when IC device receives signal (92 of fig.2) trigger signal is generated and applied to the internal clock inhibit circuits(36 of fig.3) through trigger line (60) (i.e. polling time) for initiating the operation of CPU(31) before signal demodulation start (step S1 of fig.4) and at the same time the second clock signal is applied through clock line (62) to the ROM, RAM, input/output control circuits (34)(see fig.2-4 and col.4 lines 22-42).

Re claim 27, as discussed above with respect to claim 20 and Fujioka furthermore discloses the second clock frequency from a second oscillator is higher (i.e. multiple) than first clock frequency (see col.2 lines 20-25) [i.e. second clock frequency is a multiple of the first clock frequency].

Re claim 28, as discussed above with respect to claim 27, Fujioka further discloses the second clock frequency is higher than first clock frequency (see col.2 lines 22-25).

Re claim 29, as discussed above with respect to claim 20 and Fujioka furthermore discloses the first oscillator circuits (1 of fig.2) generates first clock signal which is coupled to the CPU (31) for controlling the modulating circuits (34) for transmitting the data to the external device (see fig.2-4,col.3 lines 36-47,col.4 lines 52-58).

Re claim 32, Fujioka discloses a non-contact (i.e.contactless) IC card device (20 of fig.2) i.e. mobile data memory for data transmission with a external device (i.e. external device is able to communicate (transmit/receive) with non-contact IC card through antenna (42 of fig.2) via radio wave (91 and 92 of fig.2), therefore external device essentially functioning like read/write device) comprising: antenna circuits (42 of fig.2) for data transmitting and receiving to/from external device through antenna (42) via radio wave (91 and 92)(see fig. 2 and col.3 lines 36-48);and providing a battery component (6 of fig.2) for energy store for supplying energy consuming components includes CPU (31 of fig.2), ROM (32 RAM (33), oscillator circuits(1,2), input/output circuits (34), modulating/ demodulating circuits (41) and antenna circuits (42 of fig.2) (see fig.2-4, col.3 lines 36-63); supplying a first clock generating a lower frequency clock signal from a first oscillator for transmitting data signal to the external devices;and second oscillator generating a second higher clock frequency for reception data signal (see fig. 2-3, col.2 lines 20-25); and control unit CPU(31) intermittently connected to the number of circuits like data memory circuits ROM (32), RAM (33), oscillator circuits(1,2), input/output circuits (34), modulating/ demodulating circuits (41) and antenna circuits

(42 of fig.2),battery (6 of fig.2) for energy stored during supplying a second higher clock frequency from a second oscillator for reducing power consumption (see fig. 2-3, col.2 lines 20-25,col.3 lines36-68).

Re claim 33, as discussed above with respect to claim 32 and Fujioka furthermore discloses the non-contact IC (mobile) data memory wherein data receiver includes a data demodulator circuits(41 of fig.2) for data demodulating of a received signal from the antenna (42 of fig.2) and the data demodulator (41) is connected from the input/output control circuits(34 of fig.2), the CPU(31) and the battery (6 of fig.2) i.e. energy store device (see fig.2-4 and col.4 lines43-63).

Re claim 34, as discussed above with respect to claim 33 and Fujioka furthermore discloses the non-contact IC (mobile) data memory comprises antenna circuits (42) which includes receiver and CPU (31) [i.e. level detector] performed to judge (i.e. measure) the received data signal is correct or wrong (at step S5 of fig.4) and CPU(31) is connectable from the control circuits (34 of fig.20 and battery unit (6 of fig.2) for the energy store (see fig. 2-4 and col.5 lines 3-41) .

Re claim 35, as discussed above with respect to claim 32 and Fujioka furthermore discloses the non-contact IC (mobile) data memory comprises switching circuits (11 of fig.2) which is controlled by the CPU (31) (see fig.2-3 and col.3 lines 53-63).

Re claim 36, as discussed above with respect to claim 32 and Fujioka furthermore discloses the non-contact IC (mobile) data memory comprising a clock circuits (36 of fig. 3) i.e. timer which is controlled by CPU (31) (see fig.2-3 and col.3 lines 66-69-col.4 lines 1-5).

Re claim 37, as discussed above with respect to claim 32 and Fujioka furthermore discloses the non-contact IC (mobile) data memory comprises first clock generating oscillator and second clock generating oscillator [i.e. quartz oscillators] (see fig. 2-3 and col.2 lines20-24).

Re claim 38, Fujioka discloses an external device (i.e. external device is able to communicate (transmit/receive) with non-contact IC card through antenna (42 of fig.2) via radio wave (91 and 92 of fig.2), therefore external device essentially functioning like read/write device) comprising: antenna circuits (42 of fig.2) for data transmitting and receiving to/from external device through antenna (42) via radio wave (91 and 92)(see fig. 2 and col.3 lines 36-48);and providing a battery component (6 of fig.2) for energy store for supplying energy consuming components includes CPU (31 of fig.2), ROM (32 RAM (33), oscillator circuits(1,2), input/output circuits (34), modulating/ demodulating circuits (41) and antenna circuits (42 of fig.2) (see fig.2-4, col.3 lines36-63); supplying a first clock generating a lower frequency clock signal from a first oscillator for transmitting data signal to the external devices; and second oscillator generating a second higher clock frequency for reception data signal (see fig. 2-3, col.2 lines 20-25); and control

unit CPU(31) intermittently connected to the number of circuits like data memory circuits ROM (32), RAM (33), oscillator/clock circuits(1,2), input/output circuits (34), modulating/ demodulating circuits (41) and antenna circuits (42 of fig.2), battery (6 of. fig.2) for energy stored and connected to the second oscillator for generating second higher clock frequency for reducing power consumption (see fig. 2-3, col.2 lines 20-25,col.3 lines36-68).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim(s) 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka et al (U.S. Patent No. 5,212,373) and in view of RFID standards (ISO 1800-4 part 4, updated January 31, 2002 by Steve Halliday)

Re claim 30 and 31, Fujioka discloses all the limitations except an identification system based on the ISO/IEC 18000 standard for operation in an ISM frequency band; and the identification system is operated in an ISM frequency band of 2.45 GHz. However, RFID ISO standard teaches ISO 18000 identification systems is operated in the 2.45GHz industrial, scientific and medical (ISM) frequency bands.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made method a method for reducing the power consumption of a non-contact (i.e.contactless) IC card device i.e. mobile data memory for data transmission with a external device and higher clock frequency is used for data demodulation of a received signal (as taught by Fujioka) by standardized with the ISO

18000 radio frequency identification system can operates 2.45GHz frequency bands as taught by ISO 18000 standards to identified easily for transmit/receipt data signal by the read/write tag.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (7.96)

The following patent are cited to further show the state of the art with respect to clips and bookmarks in general:

U.S. Patent No. 6,760,578 to Rotzoll teaches wake up devices for communication system.

U.S. Patent No. 6,970,726 to Takayanagi teaches mobile station having short range radio function and power consumption reduction method.

U.S. Patent No. 6,845,454 to Kim teaches selection between high and low speed clock response.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Muhammad Akbar whose telephone number is (571)-270-1218. The examiner can normally be reached on Monday- Thursday (7:30 A.M.-5:00P.M).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MA

EDAN ORGAD
PRIMARY PATENT EXAMINER
Edan Orgad 3/31/07